Model based on-chip 13 bits ADC design dedicated to uncooled infrared focal plane arrays.

Benoit DUPONT, Patrick ROBERT, Antoine DUPRET, Patrick VILLARD, David POCHIC

ULIS, Veurey-Voroise, FRANCE
Institut d’Electronique Fondamentale, Université Paris Sud, Orsay, FRANCE
Laboratoire d’Electronique de Technologie de l’Information, Commissariat à l’Energie Atomique, Grenoble, FRANCE

ABSTRACT

This paper presents an on-chip 13 bits 10 M/S Analog to Digital Converter (ADC) specifically designed for infrared bolometric image sensor. Bolometric infrared sensors are MEMs based thermal sensors, which covers a large spectrum of infrared applications, ranging from night vision to predictive industrial maintenance and medical imaging. With the current move towards submicron technologies, the demand for more integrated, smarter sensors and microsystems has dramatically increased. This trend has strengthened the need of on-chip ADC as the interface between the analog core and the digital processing electronic. However designing an on-chip ADC dedicated to focal plane array raises many questions about its architecture and its performance requirements. To take into account those specific needs, a high level model has been developed prior to the actual design.

In this paper, we present the trade-offs of ADC design linked to infrared key performance parameters and bolometric technology detection method. The original development scheme, based on system level modeling, is also discussed. Finally we present the actual design and the measured performances.

Keywords: IRFPA, amorphous silicon, micro bolometer, uncooled IR detector, ADC

1 INTRODUCTION

Nowadays infrared sensors successfully follow a road already walked by visible light image sensors. With smaller pixel pitch, higher resolution and easier system integration, uncooled microbolometer infrared sensors intend to address new low-cost/high-volume applications such as automotive for night vision and pedestrian detections [1] [2]. Machine vision and unattended sensor also benefit from a low-cost, highly integrated infrared focal plane arrays. Thanks to deep submicron technologies, it is now possible to embed image processing, non-uniformity correction [3] or even TEC-LESS algorithms onto the silicon focal plane array. However, bolometric readout circuits remain mostly analog devices [4] [5] and the need for on-chip analog-to-digital converters has been tremendously growing in late years.

2 ARCHITECTURE

2.1 TRADE OFF IN UNCOOLED INFRARED IMAGING

Qualifying the ADC specifications begins with full understanding of infrared image sensor key figures related with the intended applications. The goal of this ADC design is to be integrated on an uncooled focal plane array. It has certain impact on the ADC design. First bolometric sensors have a very wide output dynamic from 1 to 4.2 V on a 5 V CMOS process. Noise is also an important figure for infrared imagers. The key figure of merit for infrared imager is the NETD (Noise Equivalent Temperature Difference). Achieving very low NETD values with very high operability has been achieved using uncooled bolometric infrared image sensors. It has been shown that automotive and machine vision applications can stand 80 mK NETD value [2][6]. It is critical that the ADC itself does not
downgrade the imager performance. If we consider a perfectly noise-free ADC, the inherent converter quantification noise is given by equation 1 setting the ADC noise floor.

\[
ADC_{noise} = \frac{V_{\text{dyn}}}{\sqrt{12 \cdot 2^n}}
\]  

(1)

Where \(ADC_{noise}\) is the ADC quantification noise expressed in Volts, \(V_{\text{dyn}}\) is the input dynamic range in Volts and \(n\) is the ADC’s number of bits. Therefore digital sensor \(\text{NETD}_{\text{digital}}\) can be expressed as a function of analog core \(\text{NETD}_{\text{core}}\), Responsivity \(R\) and ADC number of bits \(n\) as shown by equation 2:

\[
\text{NETD}_{\text{digital}} = \sqrt{\text{NETD}_{\text{core}}^2 + \frac{V_{\text{dyn}}^2}{12.2^{2n} R^2}}
\]

(2)

With a 500 µV RMS analog core noise, a 13 bits ADC will add quadratically 112 µV of noise. Assuming now a 75 mK bolometric technology, the use of such ADC will lead to \(\text{NETD}_{\text{digital}}\) of 78 mK provided that the ADC internal gain is equal to 1. On the contrary, a 12 bits ADC would have led to a \(\text{NETD}\) of 84 mK, which would have tighten the requirements on bolometric technology to keep \(\text{NETD}\) values below 80 mK. 4% degradation of \(\text{NETD}\) while using an internal ADC is acceptable. Finally, power consumption related to sensor floor plan is to be taken into account, as the bolometer is a thermal sensor. Therefore its response in temperature as a function of time and incident power depends on focal plane temperature as follows:

\[
C_{th} \frac{\partial(T - T_{pf})}{\partial t} = -\frac{T - T_{pf}}{R_{th}} + P_{ir}
\]

(3)

Where \(T\) is the bolometer temperature, \(T_{pf}\) the focal plane temperature, \(C_{th}\) the bolometer thermal capacitance, \(R_{th}\) its thermal resistance to the substrate and \(P_{ir}\) the incident infrared power received by each bolometer. The impact of the ADC consumption on focal plane temperature non-uniformity must be minimized.

### 2.2 ARCHITECTURE CHOICE

Visible light image sensors have experienced various solutions for analog to digital conversion [7],[8]. In certain cases, a monolithic ADC has been designed but column-wise converters are also available on particular devices [8]. With respect to the target application, the sensor features a 320x240 bolometers array on a 25 µm pixel pitch. This array is to be read out at 60 frames per second. Considering the column area dedicated to the ADC in a distributed conversion scheme it is clear based on the existing state of the art that a monolithic device would outperform the column-wise version in this particular case. Comparison figures are gathered in table 1. In fact, the distributed ADC are much more suited to very large devices and/or very high-speed cameras, which benefits from a highly parallel conversion scheme in terms of consumption and silicon occupation. This strategy has been successfully demonstrated also in visible light imagers [8] as well as in cooled infrared photovoltaic detectors [9],[10].

<table>
<thead>
<tr>
<th></th>
<th>Monolithic ADC</th>
<th>Column ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image format</td>
<td>320 x 240</td>
<td></td>
</tr>
<tr>
<td>Pixel pitch</td>
<td>25 µm</td>
<td></td>
</tr>
<tr>
<td>Imager area</td>
<td>8 mm x 6 mm</td>
<td></td>
</tr>
<tr>
<td>Frame rate</td>
<td>60Hz</td>
<td></td>
</tr>
<tr>
<td>Line rate</td>
<td>14.4 kHz</td>
<td></td>
</tr>
<tr>
<td>Column ADC area</td>
<td>1.8 mm x 0.8 mm / 1.44 mm²</td>
<td>8 mm x 0.5 mm / 4 mm²</td>
</tr>
<tr>
<td>Sensor output rate</td>
<td>4.6 MS/s</td>
<td></td>
</tr>
<tr>
<td>Conversion rate</td>
<td>4.6 MHz</td>
<td>14.4 kHz</td>
</tr>
</tbody>
</table>

Table 1: Surface and rates of column and monolithic ADCs
Various monolithic analog to digital converters have been demonstrated in imaging devices. Due to the 13 bits accuracy required for our application, we have chosen to develop a 13 bits monolithic pipeline ADC. The pipelined structure allows relatively high analog frequency with respect to 0.5 μm CMOS technology. Moreover, the accuracy can be achieved with proper capacitor matching.

3 STRUCTURE AND MODEL BASED DESIGN

3.1 ADC STRUCTURE

The ADC structure is presented on figure 1. It consists of six differential stages. Stages 1 to 5 contain a 3 bits Flash ADC. The result of each conversion is fed to a DAC, and the residual difference between the signal and the DAC output is amplified by 4 and passed to the following stage. The last stage only has 3 bits flash ADC, as there is no meaningful residual to quantify. This structure is rather classical for a pipeline ADC [11],[12]. Here one bit per stage is used as stage offset compensation using digital correction [11].

![Figure 1: Pipeline ADC structure](image1)

The main difficulty for an accurate analog to digital conversion resides in the precision of the amplification by 4 of the residual between each stage. In our approach, the subtraction of the digitized value and the amplification of the remaining voltage are realized synchronously by the circuit presented on figure 2.

![Figure 2: Detailed view of the DAC](image2)
Ash shown on figure 2, the common mode biasing is provided through the 4 Ccm capacitors bank that adapts gradually the common mode to the differential output excursion. During Phi1 Phase the proper values corresponding to the difference between the signal In+/In- and the digital stage output Bits<2.0> are stored on the capacitor bay at the input of the stage. Meanwhile, the feedback capacitors are maintained in reset while the common mode Bias is stored on Ccm capacitors. During Phi2, the residual is amplified by four and sampled by the next stage.

### 3.2 MODEL BASED DIMENSIONNING

The accuracy of such ADC resides mainly on the capacitor matching. Capacitors have to be sized generously to ensure an accurate multiplication of the residual. Increase of capacitor size leads to higher gain-bandwidth amplifiers to drive the capacitor bay the required sampling rate. To ensure proper dimensioning of the complete structure, a high level model has been developed. The model synoptic is presented on figure 4. It takes two different kinds of Inputs. Foundry inputs are necessary to take into account parameters such as amplifier noise, capacitor and transistor mismatch. It is also possible to run corner parameters. The user sets an operating frequency and chooses capacitors size, gain and bandwidth for the 5 first stages. As previously said, the last stage only features a 3 bits flash ADC. Based on the user constraints, the model computes the actual SNR, ENOB as well as the INL/DNL of the modeled ADC. Finally a THD value is calculated.

This tool bases its evaluation on extrapolated CAD simulation. To be more accurate, the modeled amplifiers are not ideal but are actually based on real schematic entry simulation under CAD tools. It is less versatile in terms of model usage. However, based on the art, first assumptions of amplifier types can be made. For instance, it is well known that most of the accuracy requirements apply on the first stages. As a consequence gain of the two first amplifiers is more likely to be higher than the following ones. A telescopic cascade with gain boost amplifier can be foreseen whereas simple cascades amplifiers may be sufficient for the last stages. However, the model keeps some level of flexibility as far as the architecture is concerned as the amplifier types can be changed with text entry.

The model helps us to tweak our design based on a 0.5 μm technology. We first estimated the dimension of the two first stages for a given ENOB. Then the last stages have been downsized using the model to lower the power consumption without degrading the ADC key figures. The model shows that the last stages capacitor area can be reduced by 60%. Amplifiers can accommodate a gain loss of 20 dB. Simulated parameters are presented in table 3.

### 4 TEST VEHICULE AND CARACTERISATION

The ADC has been first used in conjunction with a 160 x 120, 25 μm pixel-pitch, focal plane array. Figure 4 shows the floorplan of the device.
ADC has been placed as far as possible from the bolometer array to avoid thermal influence through the substrate, as explained in chapter 2.1. Specific features of the test vehicle are presented in table 2. Table 3 shows a summary of the ADC measured characteristics compared to the model output. It shows that the device model is rather accurate. There is a slight difference in THD value. The model is too optimistic. The device has been tested with the analog core and exhibit very good performances in imaging as shown on figure 5. There is no difference between digital and analog images although the scene dynamic is reduced. The ADC has been also packaged separately for characterization. The ADC has been tested at 5 MHz sampling rate with on-chip single-ended / differential converter at the input, which is the usual operating condition on the imager. DNL is below 0.67 LSB (figure 7) and most of the curve stays within +/- 0.5 LSB. The INL is 1.47 LSB (figure 8).

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.5 CMOS + A-Si microbolometers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image format</td>
<td>160 x 120</td>
</tr>
<tr>
<td>Pixel pitch</td>
<td>25 µm</td>
</tr>
<tr>
<td>NETD</td>
<td>75 mK/W (80 mK/W digital)</td>
</tr>
<tr>
<td>ADC</td>
<td>On-chip 13 bits pipeline</td>
</tr>
<tr>
<td>Digital sequencer</td>
<td>On-chip fully synchronous</td>
</tr>
<tr>
<td>Offset correction</td>
<td>On-chip skimming</td>
</tr>
<tr>
<td>User interface</td>
<td>2 wires serial programmable link</td>
</tr>
<tr>
<td></td>
<td>13 bits parallel out @ 10 MS/s max.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENOB</td>
<td>11.75</td>
<td>12.3</td>
</tr>
<tr>
<td>SNR</td>
<td>71 dB</td>
<td>74.1 dB</td>
</tr>
<tr>
<td>DNL</td>
<td>0.5</td>
<td>0.67</td>
</tr>
<tr>
<td>INL</td>
<td>1</td>
<td>1.4</td>
</tr>
<tr>
<td>THD</td>
<td>-79.3 dB</td>
<td>-73.5 dB</td>
</tr>
<tr>
<td>Power Consumption @ 5Mhz</td>
<td>73 mW</td>
<td></td>
</tr>
<tr>
<td>Power Consumption @ 10Mhz</td>
<td>115 mW</td>
<td></td>
</tr>
</tbody>
</table>

Table 2: test vehicle key features
Table 3: ADC model output and measurements
Figure 5: Infrared images with digital output (left) and analog output (right)

Figure 6: Test vehicle package

Figure 7: On-chip 13bits ADC DNL @ 5MS/s
5 CONCLUSION

In this paper, we demonstrated a focal plane array with a monolithic 13 bits ADC suitable for imaging and machine vision. The model-based development approach has also been validated as our characterization shows that the measurements are close enough from the model. The model-based design applied to the pipeline ADC allows designer to get faster and better confidence in their stage sizing. Based on this success, model based design has been extensively used at ULIS for the development of a 14 bits monolithic ADC. As stand-alone converters are suitable for small to middle size arrays, work is carried on towards the development of column-wise ADC as an R&D perspective for megapixel arrays.

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6 REFERENCES